

Low Power and Area Optimized BASK Modulators for Optical Communication

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Abstract: Binary Amplitude shift Keying (BASK) or on-off keying (OOK) is one of the digital modulation techniques in which the amplitude of carrier is changed consequently to the binary data. The conventional BASK system uses local oscillator to generate sine and cosine waves and consumes more power and area. In this paper, two new approaches are proposed to reduce area and power. The work is synthesized using cadence RTL compiler.

Keywords: BASK, OOP, WIMAX, DDFS, OFDM, AWGN and BER.

Introduction

The modulation is impressed by varying the sine and cosine inputs at a precise time. It is widely used for wireless LAN's, RFID and Bluetooth communication. BASK is used to transmit information across an optical fiber used in point to point military communication applications. Binary 1 is corresponded to a short pulse of light and 0 to the lack of light. Amplitude shift keying are not that much expensive and easily implementable. There is flaw in ASK as well, it is its sensitivity to the noise in the surrounding atmosphere, propagation circumstances and distortions. Digital satellite television broadcasters use phase-shift keying modulation of the satellite's carrier signal as part of the digital data stream encoding process. The phase-shift is the difference between the expected phase of a carrier signal and the actual phase. Most digital transmissions rely on two similar forms of phase-shift keying-8PSK and QPSK that use different modulations to encode data. QPSK uses four distinct phase to encode the data and 8PSK uses eight phases, expressed as a 3-bit number; therefore, 8PSK transmits 3-bit symbols whereas QPSK transmits 2-bit symbols per cycle. 8PSK transmits more bits per cycle compared to QPSK; it achieves a higher data rate at the same frequency than QPSK. The Low power QPSK modulator is represented in paper [1]; here the power reduction with respect to the conventional architecture is described. In the paper [2] the new approach is proposed for 16QAM modulators to reduce the power consumption. In paper [3], it is shown that the Bit Error Rate (BER) increases with increasing in the order of the modulation. In the paper [4], interference mitigation using 8PSK [10] modulation is described. In the paper [5] QPSK modulator is described with booth multiplier, booth multiplier is a digital multiplier, that replaces the analog multiplier. The output of the analog multiplier varies with the physical parameter variation such as temperature. Digital multiplier is advantageous in terms of speed and power. In the paper [6] BER analysis are performed using different modulation techniques over AWGN, Rayleigh and Rician channels with and without OFDM model. In the paper [7], the DDFS (Digital Direct Frequency Synthesizer) is described. The synthesizer consumes less area compared to the conventional synthesizer. In this paper, two new approaches are proposed. These two approaches are described as below. The paper is organized as three parts. First part explains the conventional BASK modulator. The second part explains BASK modulator with iterative algorithm and Third part explains the proposed BASK modulator based on carrier data storage in memory. Finally results are compared and discussed.

Conventional BASK Modulator

The conventional BASK modulator is shown in Figure.1, Input binary data is encoded, the NRZ encoder output is applied to the multiplier. The carrier generated using local oscillator is multiplied with the information bit to generate BASK signal as shown in Figure1.

Proposed BASK Modulator with Iterative algorithm

The proposed BASK modulator using iterative based algorithm is shown below in Figure.2, the carrier data is generated. The generated sine data is multiplied with the NRZ level encoder output. The sine and cosine data are computed as represented in the following equations (1) and (2) respectively.

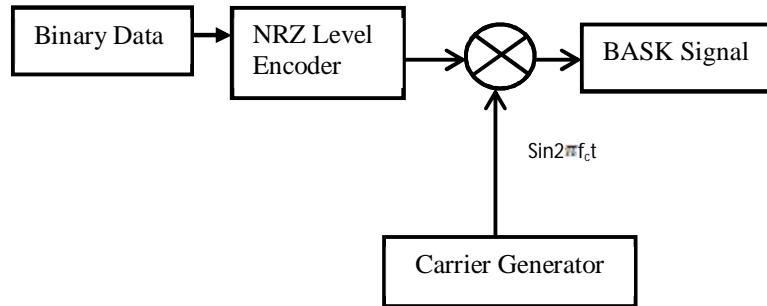


Figure1. Conventional BASK Modulator

$$\text{sine} = \text{sine_reg} + \{\text{cos_reg}[n], \text{cos_reg}[n], \text{cos_reg}[n], \text{cos_reg}[n:m]\} \tag{1}$$

$$\text{cos} = \text{cos_reg} - \{\text{sine}[n], \text{sine}[n], \text{sine}[n], \text{sine}[n:m]\} \tag{2}$$

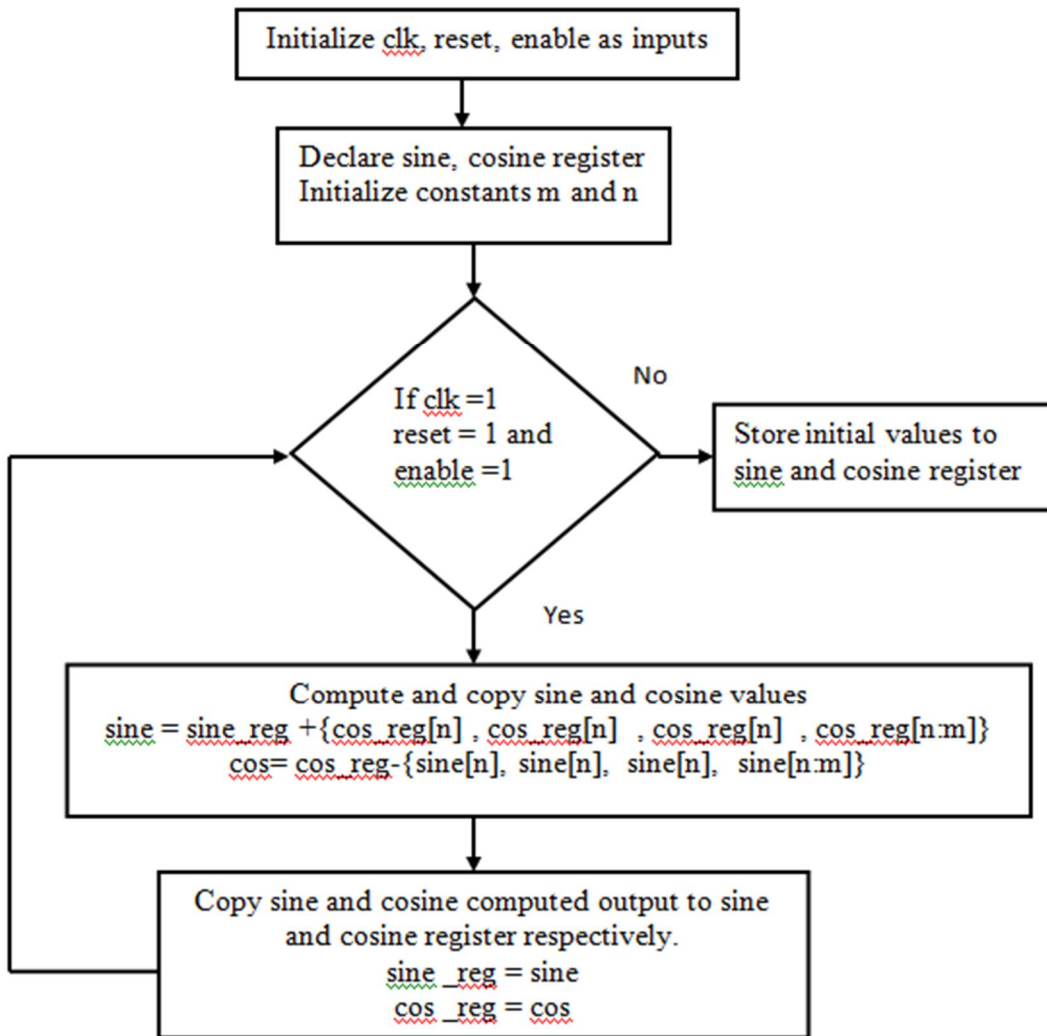


Figure2. Generation of sine and cosine data

Proposed BASK Modulator-2

The carrier data generated from the above method is stored in memory. If the data sequence is logic ‘1’ the carrier data is selected. The proposed BASK modulator-2 is shown in Figure.3.

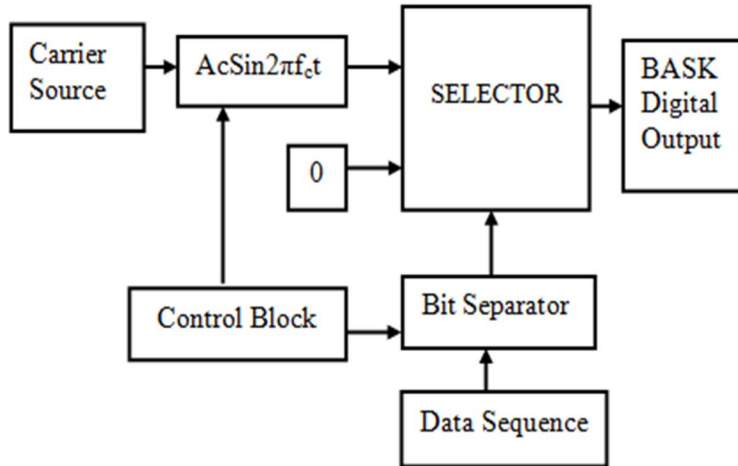


Figure.3. Proposed BASK Modulator-2

Result and Analysis

Synthesis report of Conventional Method:

- **Xilinx Synthesis Report**

The RTL, technology schematic of conventional BASK modulator is represented in Figure.4 and simulation outcome of conventional BASK Modulator is shown in Figure 4 and 5.

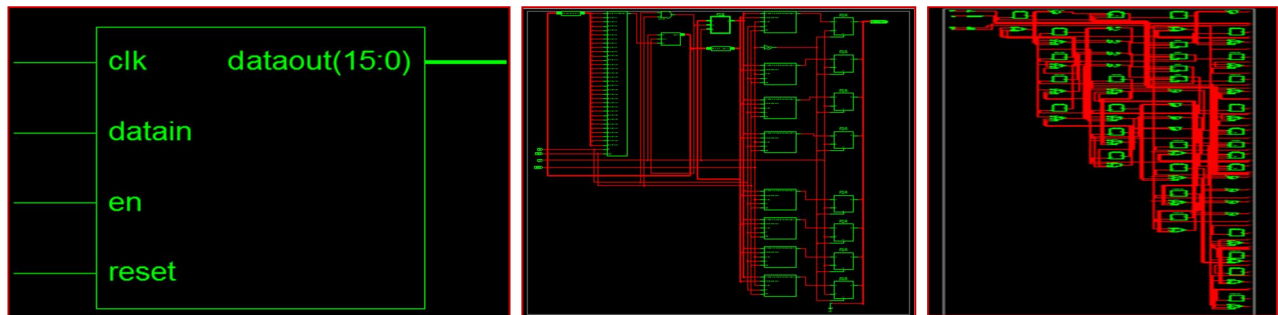


Figure 4. RTL and Technology schematic of conventional BASK Modulator

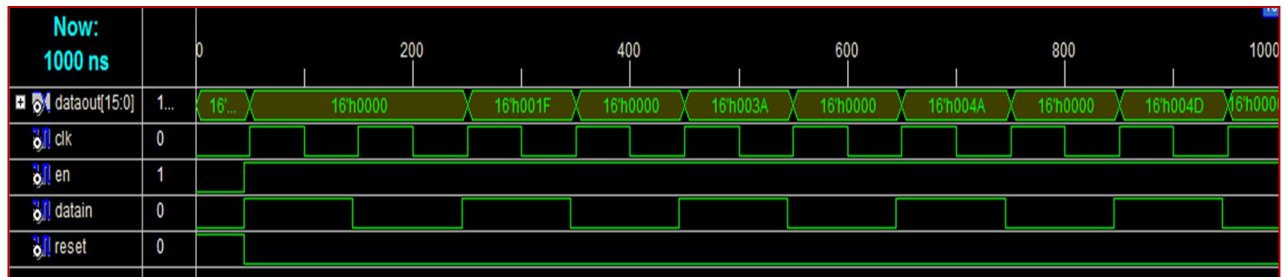


Figure 5. Simulation results of conventional BASK Modulator

- **Cadence synthesis Report**

Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology is shown in Figure 6. Power and area report of conventional BASK modulator in 180nm, 90nm and 45nm technology is represented in Table1.

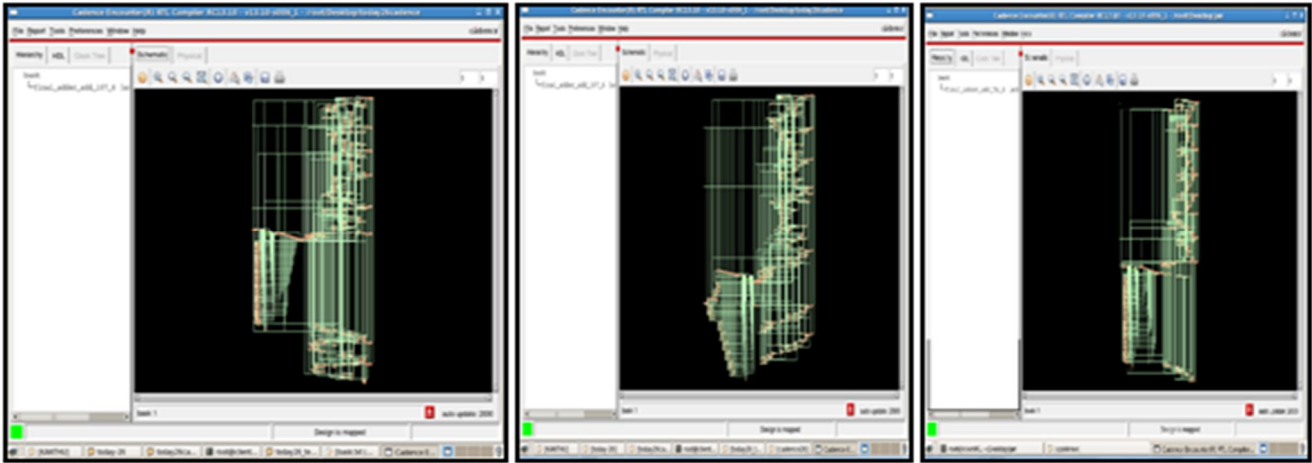


Figure. 6. Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology

Table 1.Area and Power report of BASK with conventional method

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total area (μm^2)
180nm	475	218.127	172645.65	172863.8	8911
90nm	475	11626.951	38614.244	50241.2	2878
45nm	446	352.032	10832.730	11184.8	686

Synthesis Report of BASK with Iterative Algorithm

• **Xilinx Synthesis Report**

RTL, Technology and simulation results of BASK modulator with proposed algorithm-2 is made known in Figure 7 and 8 below.

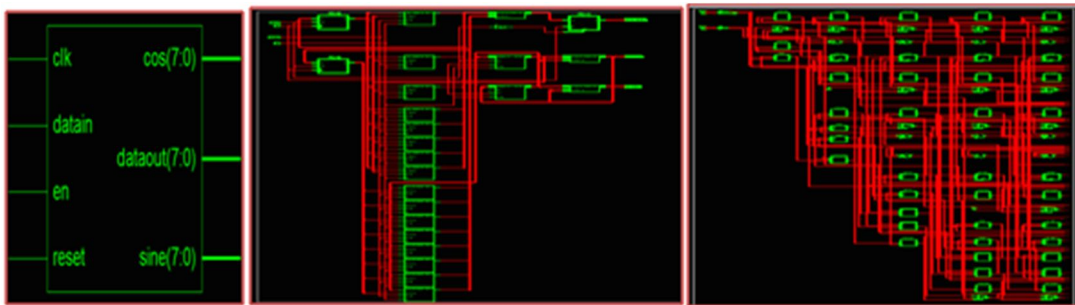


Figure 7. RTL and Technology schematic of BASK Modulator with Iterative Algorithm

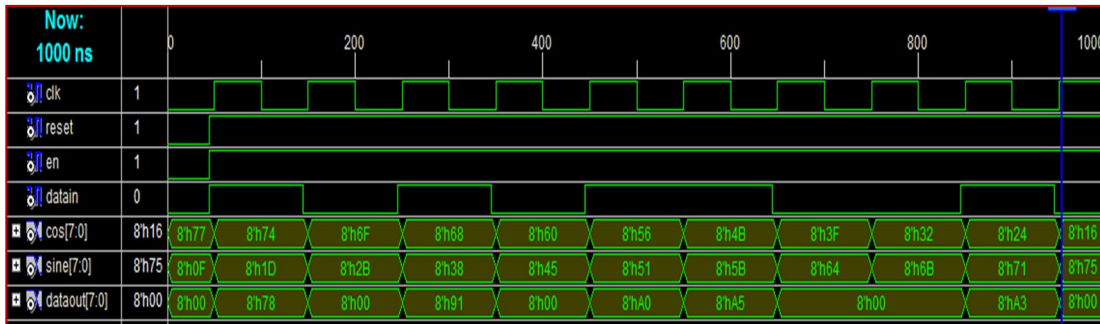


Figure 8.Simulation results of BASK Modulator with Proposed Iterative Algorithm-2

Cadence synthesis Report

Synthesis Report of Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology is shown in Figure.9. Power, Area and Gate report of proposed BASK modulator with proposed algorithm-2 in 180nm, 90nm and 45nm technology is mentioned in the Table2 respectively.

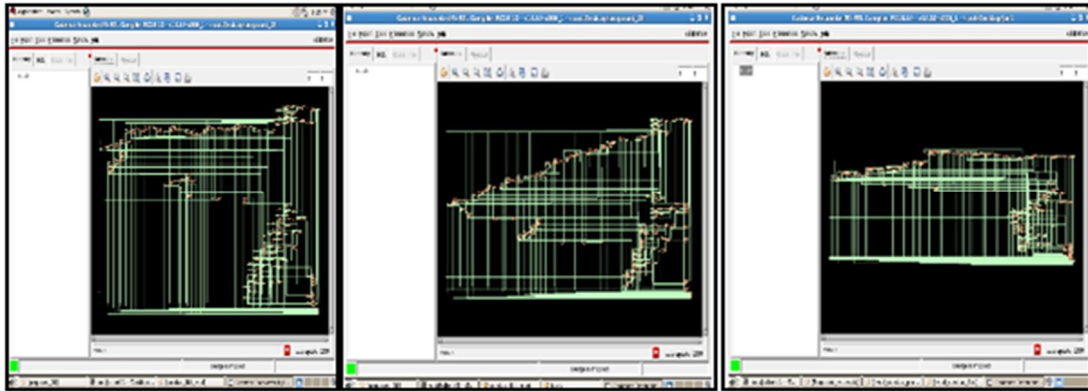


Figure 9. Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology

Table 2. Area and Power report of BASK with Iterative algorithm

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total area (μm^2)
180nm	148	165.869	209031.6	209197.5	5039
90nm	141	8377.552	47731.22	56108.8	1555
45nm	195	242.244	8286.392	8528.63	435

Proposed BASK-Modulator-2

Xilinx synthesis Report Proposed BASK Modulator-2

RTL, technology schematic and simulation results of BASK Modulator-2 is revealed in Figure.10 and Figure.11 below.

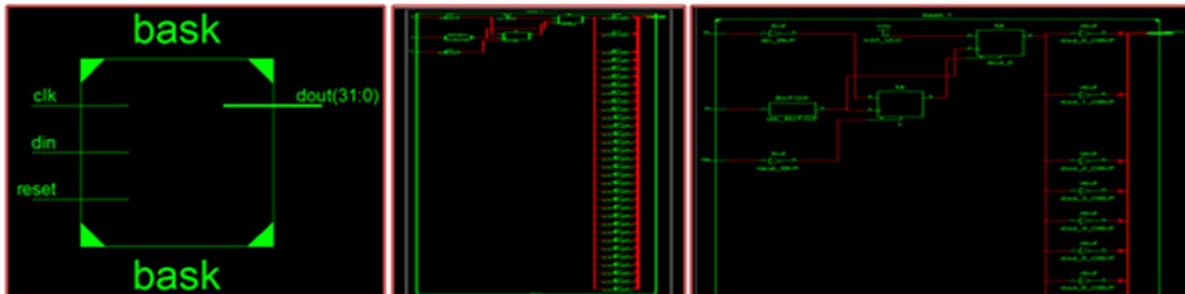


Figure 10. RTL and Technology schematic of BASK Modulator -2

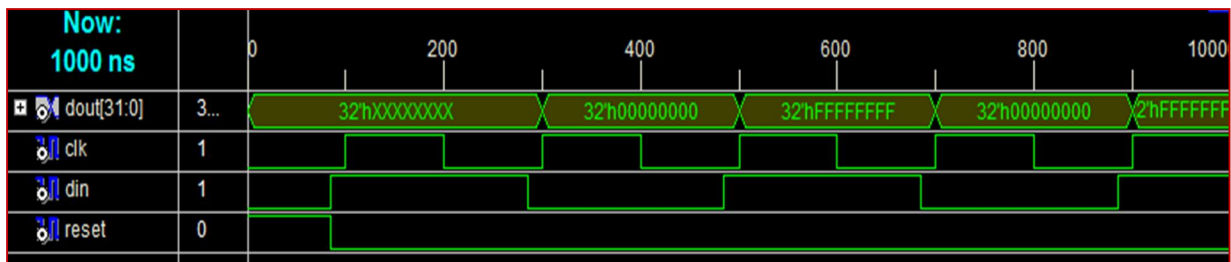


Figure 11. Simulation results of proposed BASK Modulator-2

• Cadence synthesis Report

Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology is shown in Figure.12. Power, area and gate report of proposed BASK modulator-2 in 180nm, 90nm and 45nm technology is indicated in Table3.

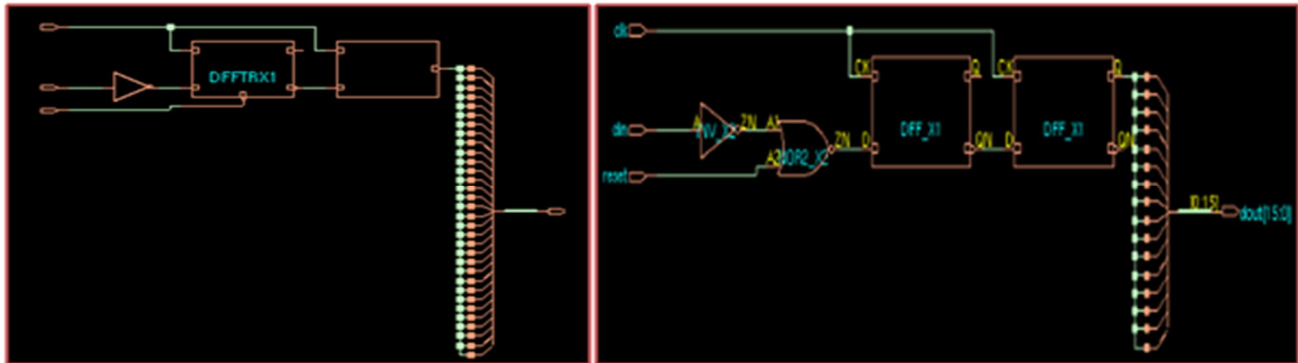


Figure 12. Cadence Encounter(R) RTL Compiler RC13.10-v13.10-s006_1 output in 180nm, 90nm and 45nm technology

Table 3.Area and Power report of BASK Modulator-2

Technology	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)	Total area (μm^2)
180nm	3	3.521	3572.658	3576.179	116
90nm	3	221.421	901.512	1122.933	39
45nm	4	6.627	361.635	368.262	11

• Device utilization of proposed modulators with Conventional BASK modulator

The device utilization of proposed BASK modulators with conventional BASK modulator as shown in Figure 13.

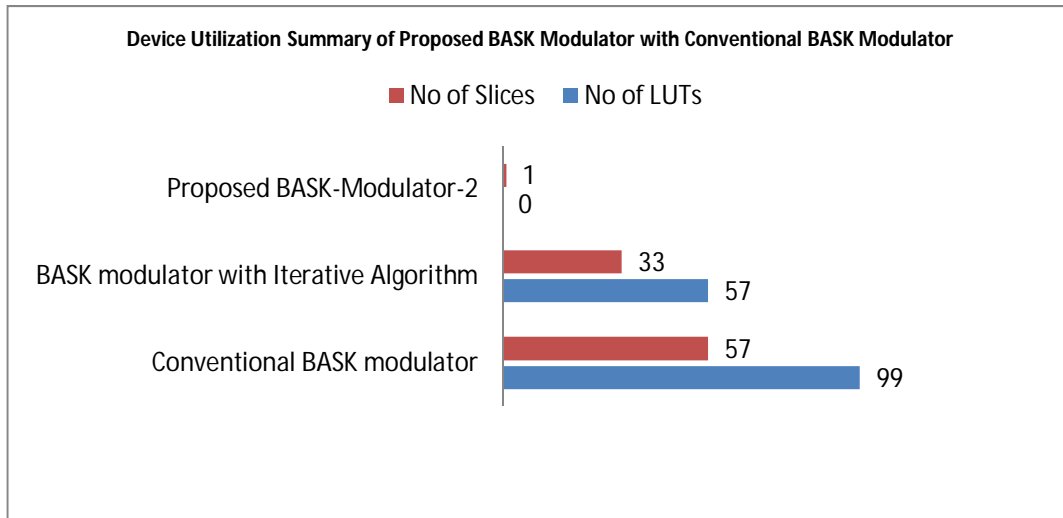


Figure 13. Device utilization of conventional BASK Modulator with proposed Methods

It has shown that the device utilization is more in conventional BASK modulator compared to proposed BASK modulators as displayed in Figure 13.

• Power Comparison Report of BASK Modulators

The power comparison report of conventional BASK modulator with proposed modulators as shown in Figure 14. The power consumption is more in BASK modulator with iterative algorithm and minimized in proposed BASK modulator-2. The power report in 180nm, 90nm and 45nm technology is shown in Figure14 below.

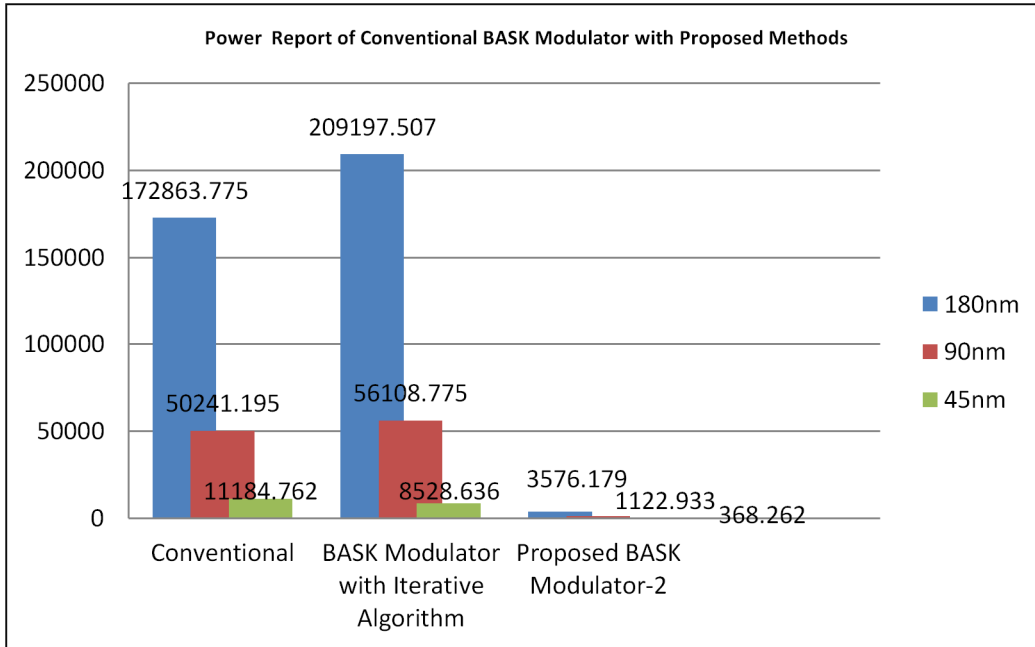


Figure 14. Power comparison report of BASK modulators

- Area Comparison of BASK Modulators**

The area comparison report of conventional BASK modulator with proposed modulators as shown in Figure 15. The area report utilization is more in conventional BASK modulator in comparison with the proposed modulators. The proposed BASK modulator-2 utilizes less area as indicated in Fig.15 below in 180nm, 90nm and 45nm CMOS technologies.

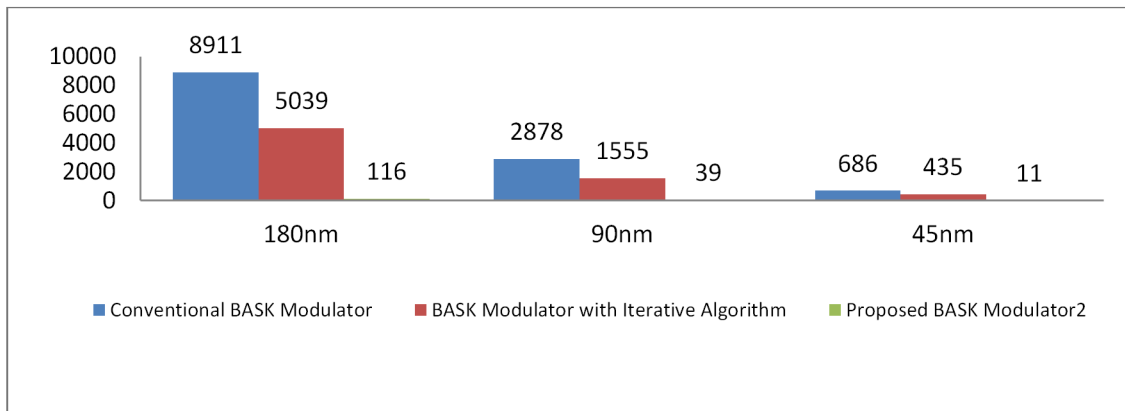


Figure 15. Area comparison report of BASK modulators

Conclusion

In this work, the BASK modulator is synthesized using cadence RTL compiler, the power consumption and area utilization report in reported in 180nm, 90nm and 45nm technology. The less power consumption and area reduction is achieved compared to conventional BASK modulator.

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